

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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SWITCHING

P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ673 is P-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ673	Isolated TO-220 (MP-45F)

FEATURES

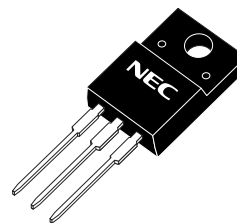
- Super low on-state resistance

$R_{DS(on)1} = 20 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -18 \text{ A)}$

$R_{DS(on)2} = 31 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -18 \text{ A)}$

- Low C_{iss} : $C_{iss} = 4600 \text{ pF TYP.}$
- Built-in gate protection diode

(Isolated TO-220)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	∓ 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	∓ 36	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	∓ 144	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	32	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	-36	A
Single Avalanche Energy ^{Note2}	E_{AS}	130	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = -30 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

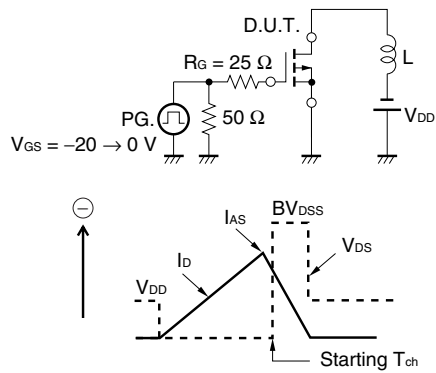
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ELECTRICAL CHARACTERISTICS (TA = 25°C)

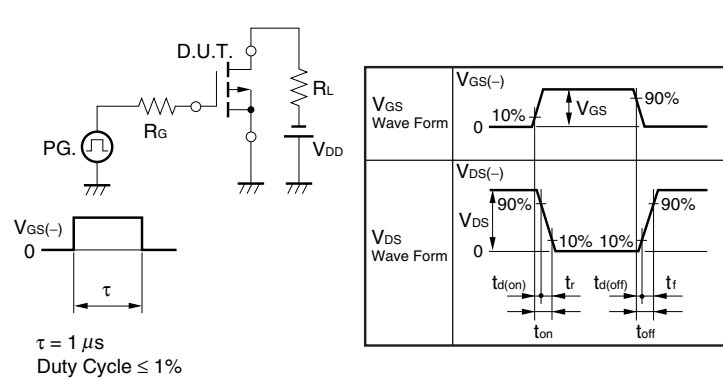
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$			-10	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			∓ 10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-1.5	-2.0	-2.5	V
Forward Transfer Admittance ^{Note}	$ y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -18\text{ A}$	22			S
Drain to Source On-state Resistance ^{Note}	$R_{DS(on)1}$	$V_{GS} = -10\text{ V}, I_D = -18\text{ A}$		17	20	$\text{m}\Omega$
	$R_{DS(on)2}$	$V_{GS} = -4.0\text{ V}, I_D = -18\text{ A}$		22	31	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}$		4600		pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$		820		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1\text{ MHz}$		330		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -30\text{ V}, I_D = -18\text{ A}$		14		ns
Rise Time	t_r	$V_{GS} = -10\text{ V}$		14		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 0\ \Omega$		130		ns
Fall Time	t_f			50		ns
Total Gate Charge	Q_G	$V_{DD} = -48\text{ V}$		87		nC
Gate to Source Charge	Q_{GS}	$V_{GS} = -10\text{ V}$		15		nC
Gate to Drain Charge	Q_{GD}	$I_D = -36\text{ A}$		22		nC
Body Diode Forward Voltage ^{Note}	$V_{F(S-D)}$	$I_F = -36\text{ A}, V_{GS} = 0\text{ V}$		1.0		V
Reverse Recovery Time	t_{rr}	$I_F = -36\text{ A}, V_{GS} = 0\text{ V}$		52		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{ A}/\mu\text{s}$		84		nC

Note Pulsed

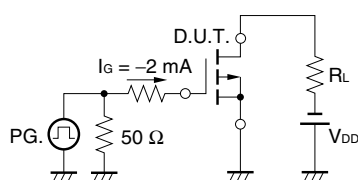
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

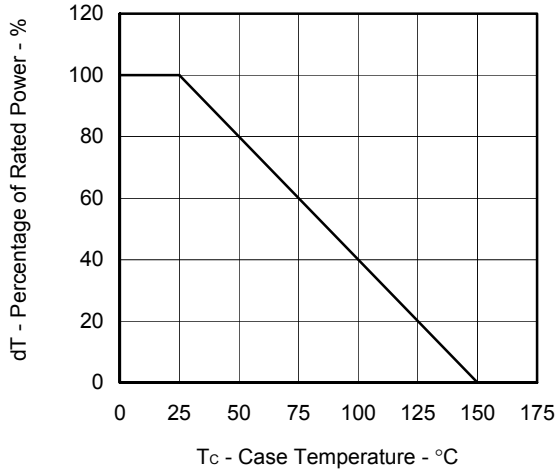


TEST CIRCUIT 3 GATE CHARGE

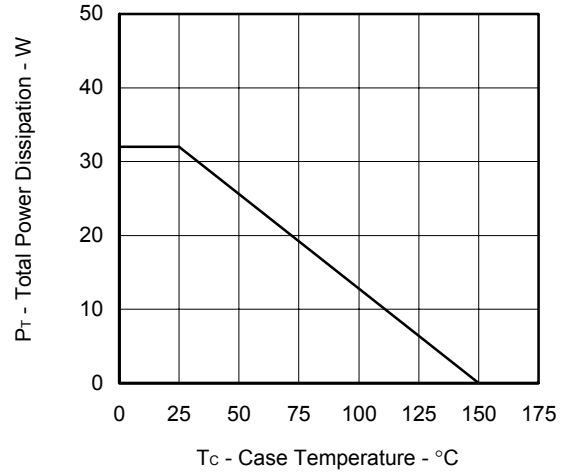


TYPICAL CHARACTERISTICS (T_A = 25°C)

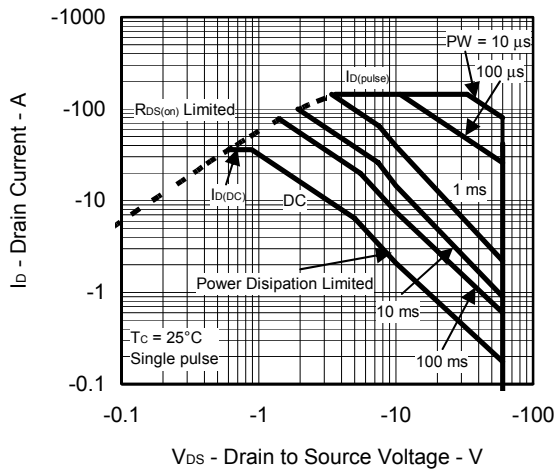
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



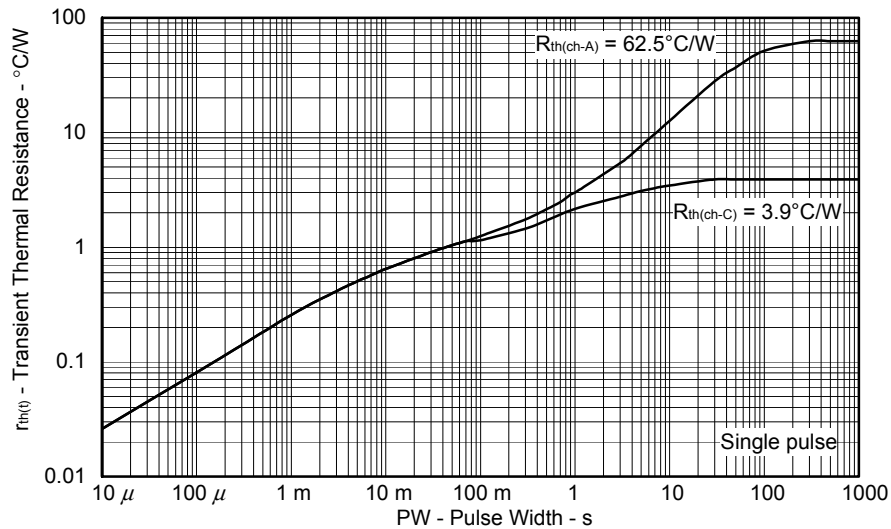
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



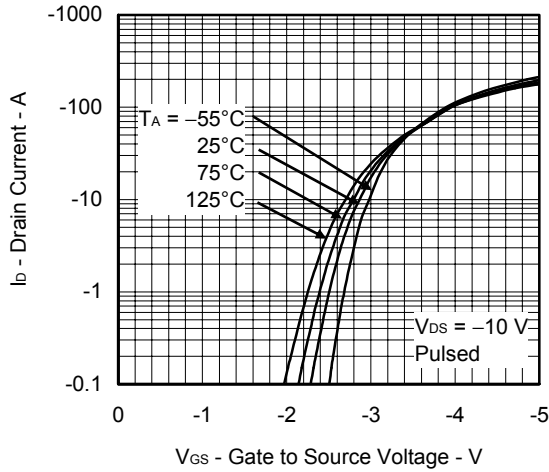
FORWARD BIAS SAFE OPERATING AREA



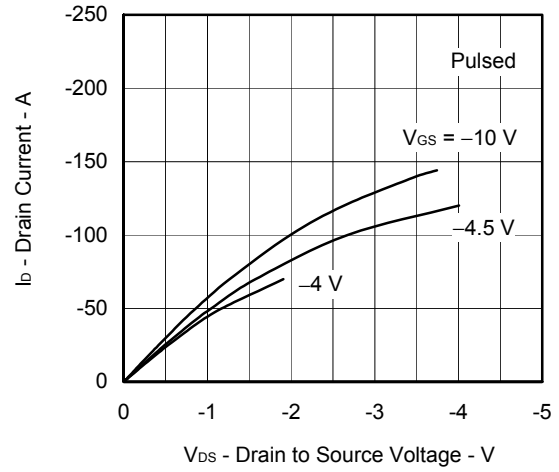
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



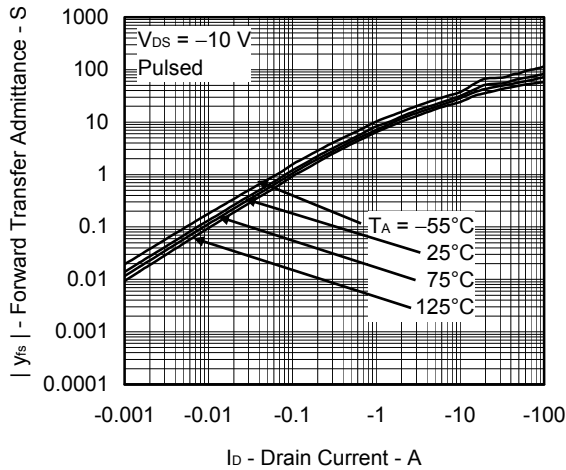
FORWARD TRANSFER CHARACTERISTICS



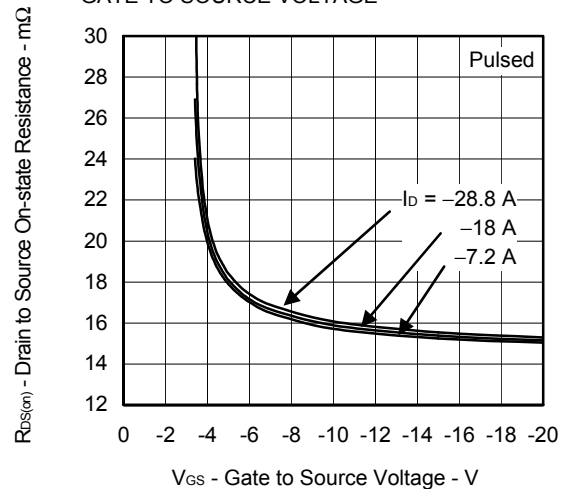
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



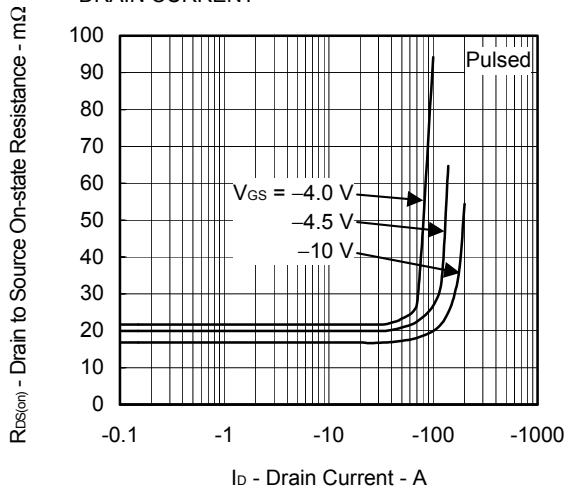
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



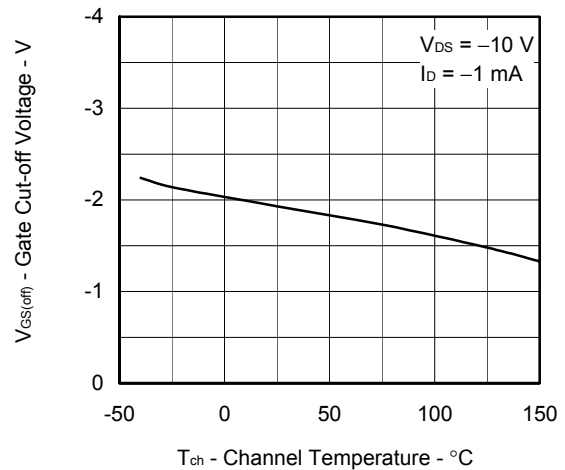
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



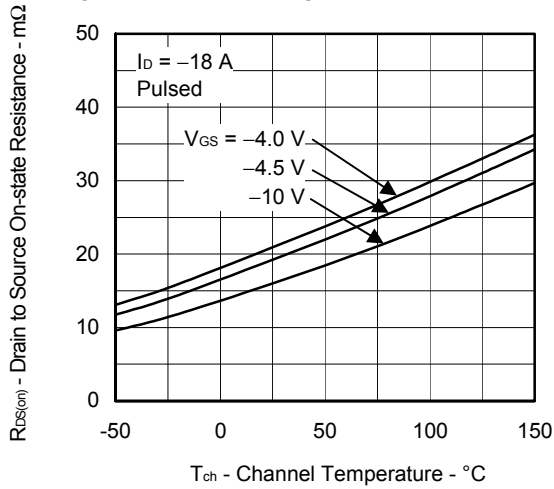
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



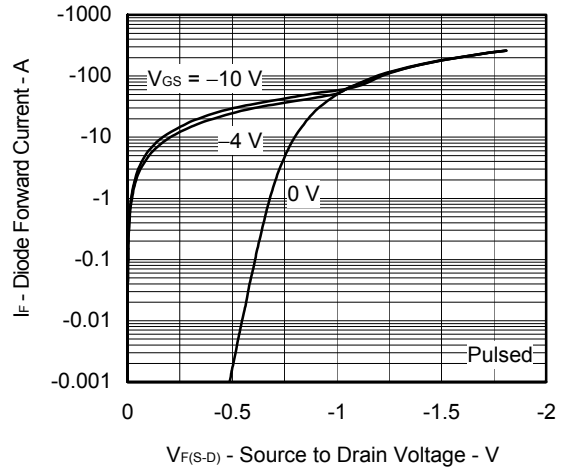
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



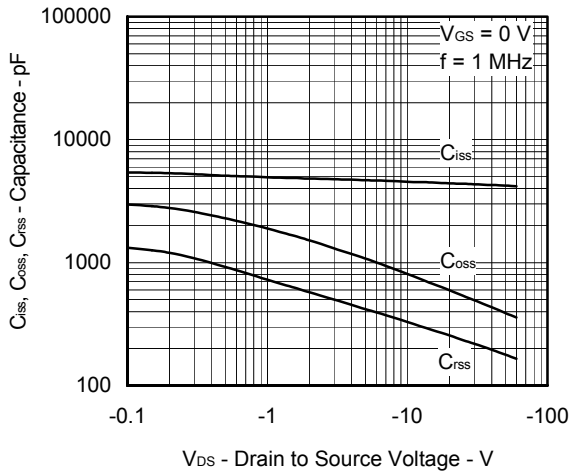
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



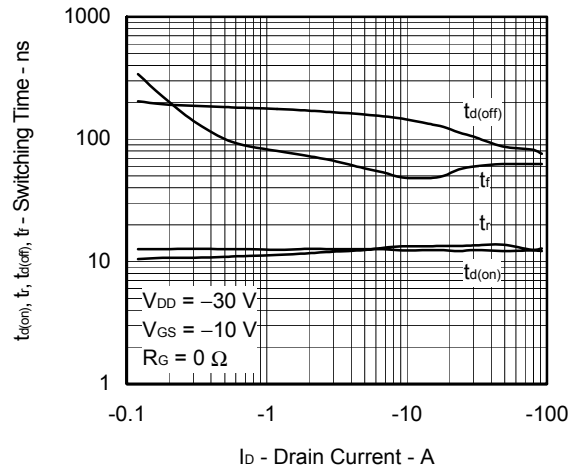
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



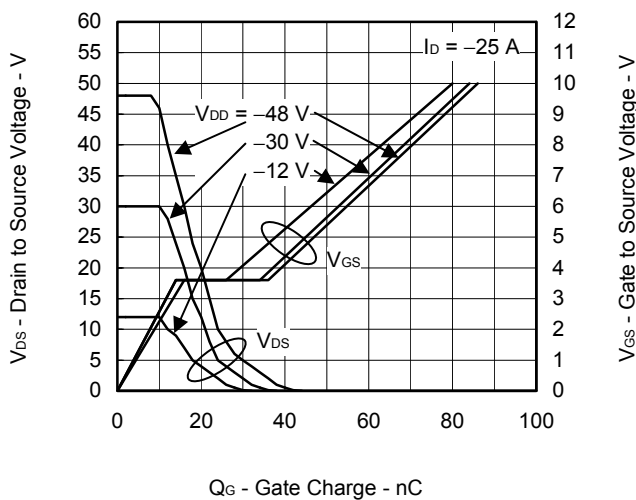
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



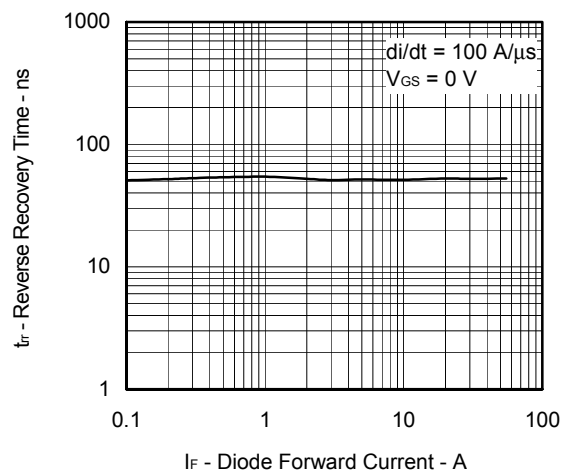
SWITCHING CHARACTERISTICS



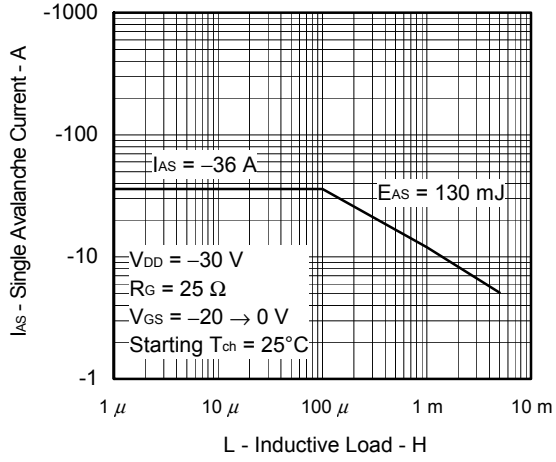
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



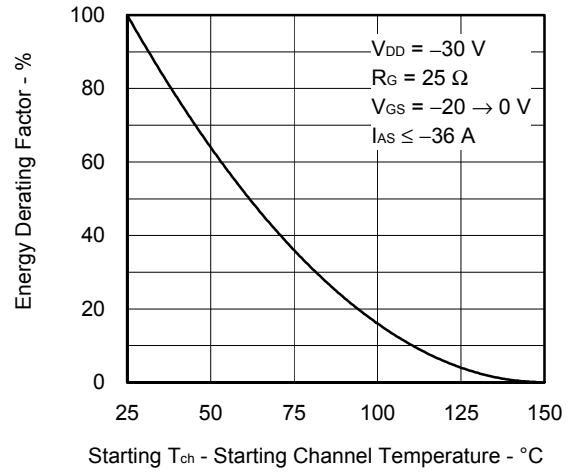
SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

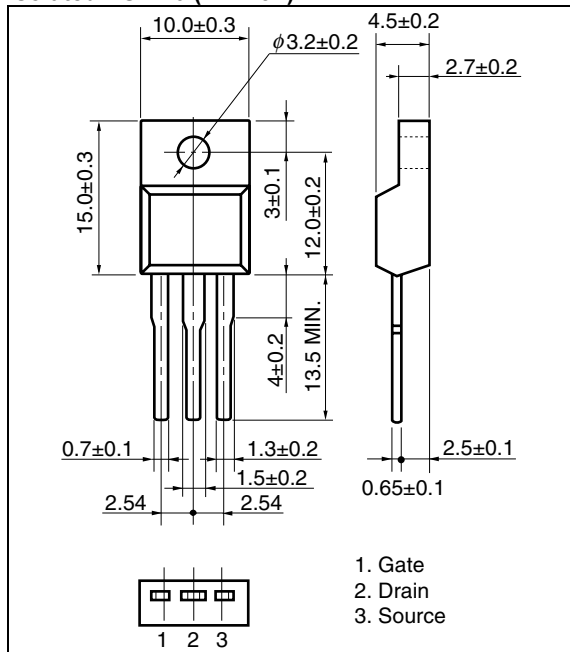


SINGLE AVALANCHE ENERGY DERATING FACTOR

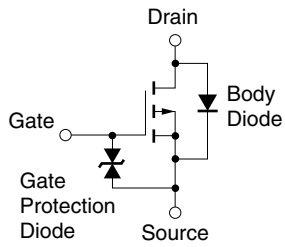


PACKAGE DRAWING (Unit: mm)

Isolated TO-220 (MP-45F)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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