

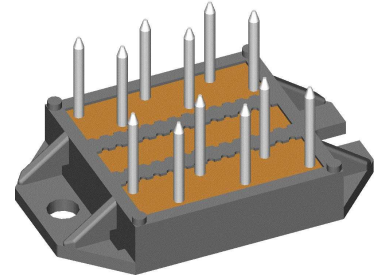
Thyristor Module

$V_{RRM} = 800\text{ V}$
 $I_{TAV} = 16\text{ A}$
 $V_T = 1.19\text{ V}$

AC Controlling
3~ full-controlled

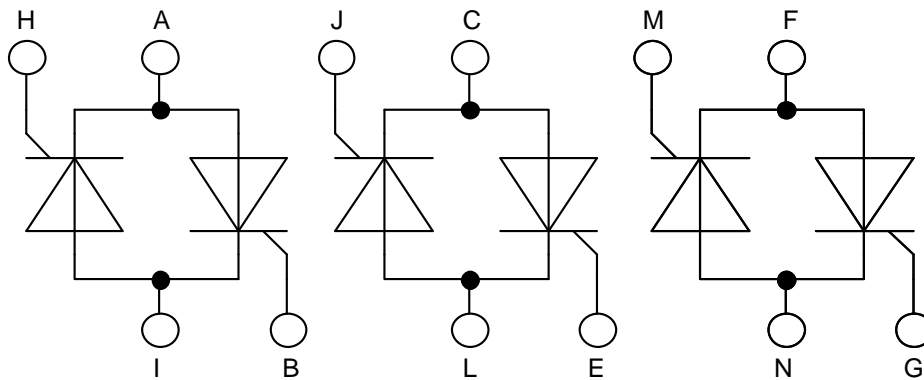
Part number

VWO35-08H07



Backside: isolated

E72873



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Direct Copper Bonded Al₂O₃-ceramic

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: ECO-PAC1

- Isolation Voltage: 3000 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Height: 9 mm
- Base plate: DCB ceramic
- Reduced weight
- Advanced power cycling

Terms Conditions of usage:

The data contained in this product data sheet is exclusively intended for technically trained staff. The user will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to his application. The specifications of our components may not be considered as an assurance of component characteristics. The information in the valid application- and assembly notes must be considered. Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of your product, please contact your local sales office.

Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact your local sales office.

Should you intend to use the product in aviation, in health or life endangering or life support applications, please notify. For any such application we urgently recommend

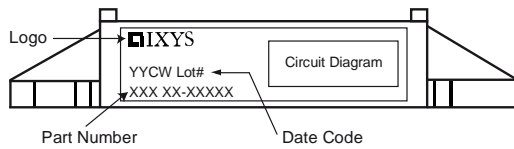
- to perform joint risk and quality assessments;

- the conclusion of quality agreements;

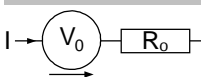
- to establish joint measures of an ongoing product survey, and that we may make delivery dependent on the realization of any such measures.

Rectifier				Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit	
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			900	V	
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			800	V	
I_{RD}	reverse current, drain current	$V_{R/D} = 800 V$	$T_{VJ} = 25^{\circ}C$		50	μA	
		$V_{R/D} = 800 V$	$T_{VJ} = 125^{\circ}C$		2	mA	
V_T	forward voltage drop	$I_T = 15 A$	$T_{VJ} = 25^{\circ}C$		1.23	V	
		$I_T = 30 A$			1.48	V	
		$I_T = 15 A$	$T_{VJ} = 125^{\circ}C$		1.19	V	
		$I_T = 30 A$			1.51	V	
I_{TAV}	average forward current	$T_C = 85^{\circ}C$	$T_{VJ} = 125^{\circ}C$		16	A	
I_{RMS}	RMS forward current per phase	180° sine			35	A	
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 125^{\circ}C$		0.88	V	
r_T	slope resistance				21	m Ω	
R_{thJC}	thermal resistance junction to case				1.3	K/W	
R_{thCH}	thermal resistance case to heatsink			0.500		K/W	
P_{tot}	total power dissipation		$T_C = 25^{\circ}C$		77	W	
I_{TSM}	max. forward surge current	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		200	A	
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		215	A	
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 125^{\circ}C$		170	A	
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		185	A	
I^2t	value for fusing	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		200	A ² s	
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		190	A ² s	
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 125^{\circ}C$		145	A ² s	
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		140	A ² s	
C_J	junction capacitance	$V_R = 400 V \quad f = 1 \text{ MHz}$	$T_{VJ} = 25^{\circ}C$		7	pF	
P_{GM}	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 125^{\circ}C$		5	W	
		$t_p = 300 \mu s$			2.5	W	
P_{GAV}	average gate power dissipation				0.5	W	
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 125^{\circ}C; f = 50 \text{ Hz}$	repetitive, $I_T = 45 A$		100	A/ μs	
		$t_p = 200 \mu s; di_G/dt = 0.15 A/\mu s;$	non-repet., $I_T = 15 A$		500	A/ μs	
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^{\circ}C$		500	V/ μs	
		$R_{GK} = \infty; \text{method 1 (linear voltage rise)}$					
V_{GT}	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		1.5	V	
			$T_{VJ} = -40^{\circ}C$		2.5	V	
I_{GT}	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		25	mA	
			$T_{VJ} = -40^{\circ}C$		50	mA	
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^{\circ}C$		0.2	V	
I_{GD}	gate non-trigger current				3	mA	
I_L	latching current	$t_p = 10 \mu s$	$T_{VJ} = 25^{\circ}C$		75	mA	
		$I_G = 0.1 A; di_G/dt = 0.1 A/\mu s$					
I_H	holding current	$V_D = 6 V \quad R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		50	mA	
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	μs	
		$I_G = 0.1 A; di_G/dt = 0.1 A/\mu s$					
t_q	turn-off time	$V_R = 100 V; I_T = 15 A; V = \frac{2}{3} V_{DRM}$	$T_{VJ} = 100^{\circ}C$		150	μs	
		$di/dt = 10 A/\mu s \quad dv/dt = 20 V/\mu s \quad t_p = 200 \mu s$					

Package ECO-PAC1				Ratings		
Symbol	Definition	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal			40	A
T_{VJ}	virtual junction temperature		-40		125	°C
T_{op}	operation temperature		-40		100	°C
T_{stg}	storage temperature		-40		125	°C
Weight					19	g
M_D	mounting torque		1.4		2	Nm
$d_{Spp/App}$	creepage distance on surface striking distance through air	terminal to terminal	6.0			mm
$d_{Spb/Apb}$		terminal to backside	10.0			mm
V_{ISOL}	isolation voltage	t = 1 second	3000			V
		t = 1 minute	2500			V

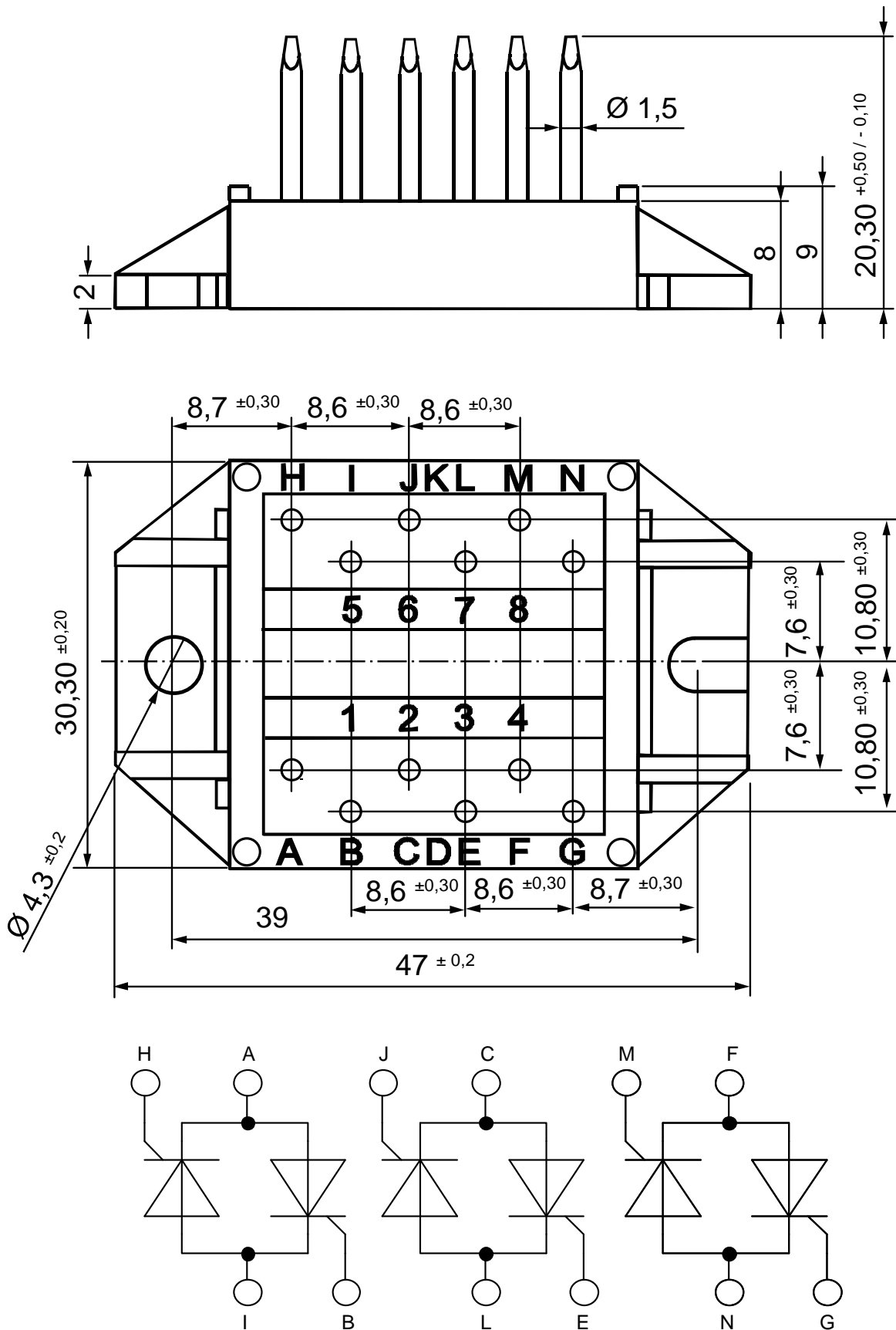


Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	VWO35-08HO7	VWO35-08HO7	Box	25	491837

Equivalent Circuits for Simulation
** on die level*
 $T_{VJ} = 125\text{ °C}$

Thyristor

$V_{0\ max}$	threshold voltage	0.88	V
$R_{0\ max}$	slope resistance *	18	mΩ

Outlines ECO-PAC1



Thyristor

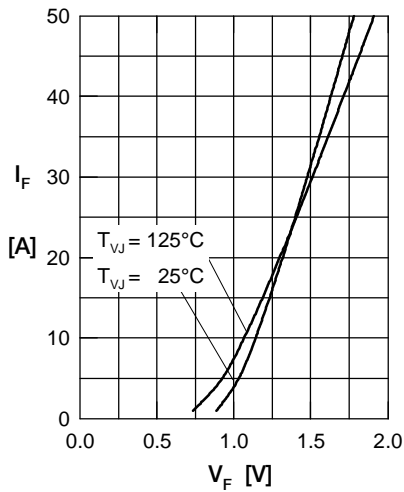


Fig. 1 Forward current vs. voltage drop per thyristor

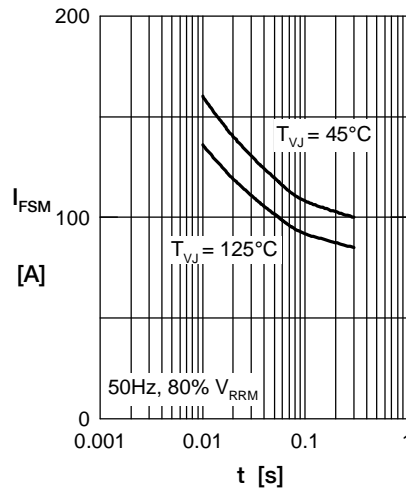


Fig. 2 Surge overload current vs. time per thyristor

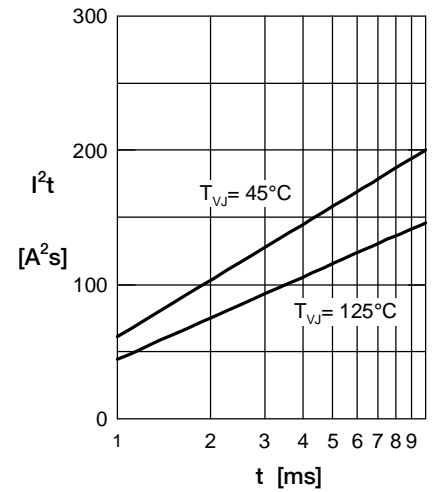


Fig. 3 I^2t vs. time per thyristor

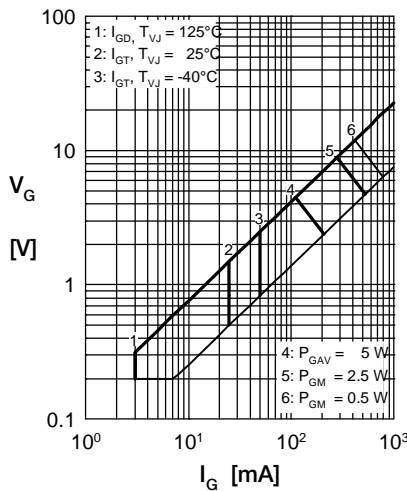


Fig. 4 Gate trigger characteristics

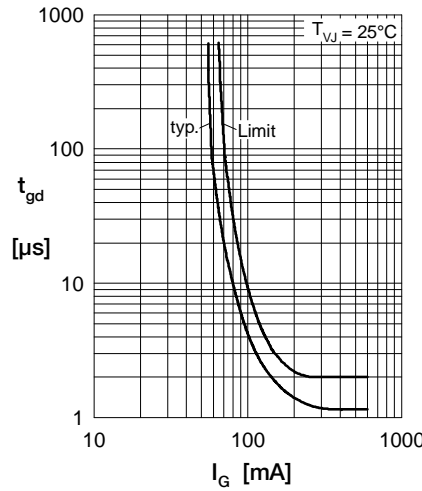


Fig. 5 Gate trigger delay time

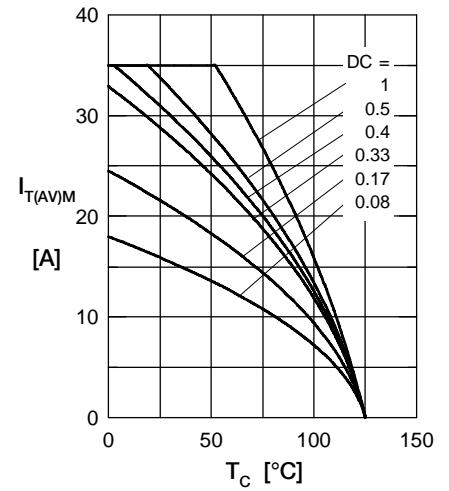


Fig. 5 Max. forward current vs. case temperature per thyristor

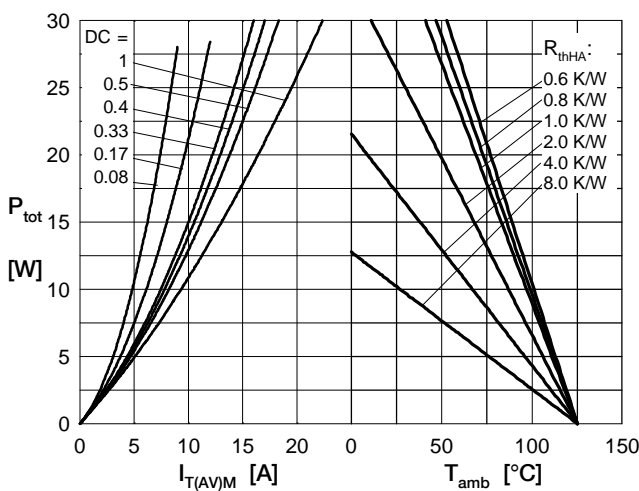


Fig. 4 Power dissipation vs. forward current and ambient temperature per thyristor

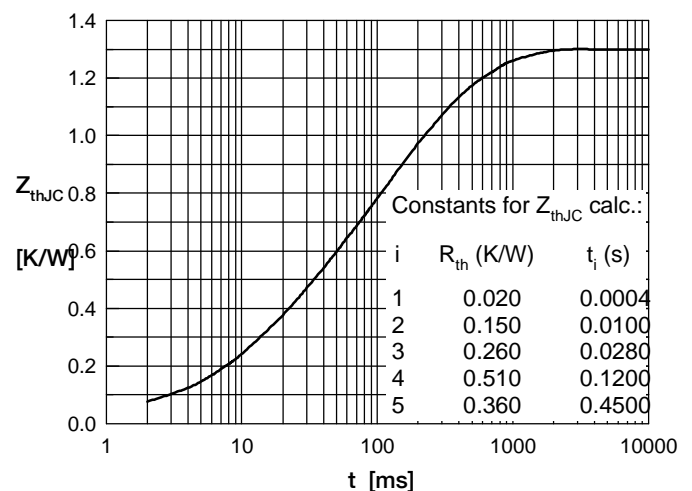


Fig. 6 Transient thermal impedance junction to case vs. time per thyristor